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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,597	08/04/2003	Uri Cummings	FULCP009	6534

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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/634,597	CUMMINGS ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,11-13,15,18,19,24 and 31-37* is/are rejected.

7)☒ Claim(s) *2-10,14,16,17,20-23 and 25-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed on 04/05/2005 has been entered. Claims 1-37 are pending in this Office action.

Response to Arguments

2. Applicant's arguments, see pages 10-11 under Remarks, filed on 04/05/2005, with respect to the rejection(s)of claim(s) 1, 11-13, 15, 18-24, 27 and 31-37 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Wicki et al. U.S. Patent 5,838,684.

3. The objection of claims 5 and 8 has been withdrawn after Applicants clarifies the scope of claims 5 and 8.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 11-13, 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wicki et al. U.S. Patent 5,838,684.

Regarding claim 1, Wicki et al. invention is directed to a plesio-asynchronous and asynchronous router circuit 3 as shown in figure 1. In column 10, lines 20-45, Wicki et al. teaches a router circuit, corresponding to the claimed integrated circuit, for communicating with neighboring circuits, comprises:

A plurality of inputs ports for receiving frames of data. Further in column 4, lines 30-40, the router system 3 includes a mesh link clock domain 110 per input port. Figure 6 further shows details of input port 604i. Wicki et al. does not show a plurality of synchronous modules as set forth in the application claim. As recited above, router circuit 3 communicates with neighboring circuits, wherein each of neighboring circuits has a clock domain 110. Hence, each neighboring circuit is synchronous module, each having a data rate.

Wicki et al. does not disclose a plurality of clock domain converters as set forth in the application claim. Nevertheless, in column 2, lines 20-30, in one embodiment, frame transmission is asynchronous and the router system is not synchronous. Frames arrives at one clock is clocked out with another clock. Furthermore, in column 5, lines 1-25, the input buffer synchronizes data from the incoming clock to the local clock domain, and by receiving input data according to input clock signal and by producing data with output clock signal. Therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention that the input buffer acts as a clock converter for converting frames between one clock domain of corresponding synchronous module and an

asynchronous domain via the router system according to an asynchronous handshake protocol.

As disclosed in Wicki invention, the router system is not synchronous and the router system 3 includes a crossbar switch as shown in figure 144' without internal blocking, providing a dedicated connection to the crossbar for each buffer element of the input buffers; see column 2, lines 35-60. In view of that, the crossbar switch is asynchronous crossbar switch. Furthermore, in column 10, lines 30-40, the crossbar switch has a plurality of inputs and outputs, each input buffer coupled to an input of the crossbar switch to the input buffer, each output port coupled to an output of the crossbar switch dedicated to the output port, the crossbar switch for switchably coupling any input buffer to any output port to implement FIFO channel; see also column 5, lines 40-60.

Regarding claim 11, as recited above, the crossbar switch has a plurality of inputs and outputs, each input buffer coupled to an input of the crossbar switch to the input buffer, each output port coupled to an output of the crossbar switch dedicated to the output port, the crossbar switch for switchably coupling any input buffer to any output port according to the routing information in each frame header. The routing events are uncorrelated.

Regarding claim 12, crossbar unit 30 in figure 3 is inherently operable to transfer data based on the local clock domain. In column 4, lines 35-43, according to one

embodiment, the router system 3 can operate with a clock frequency of 200 Mhz and beyond for multiprocessor interconnects.

Regarding claim 13, as recited in claim 12, the router system 3 can operate with a clock frequency of 200 Mhz and beyond for multiprocessor interconnects. Therefore, the timing assumption is pulse-timing assumption.

Regarding claim 15, as recited in claim 1, crossbar switch as shown in figure 144' without internal blocking, providing a dedicated connection to the crossbar for each buffer element of the input buffers. Therefore, the asynchronous handshaking is delay-insensitive.

Regarding claim 18, as recited in claim 1, in column 10, lines 30-40, the crossbar switch has a plurality of inputs and outputs, each input buffer coupled to an input of the crossbar switch to the input buffer, each output port coupled to an output of the crossbar switch dedicated to the output port, the crossbar switch for switchably coupling any input buffer to any output port, therefore, the crossbar switch can arbitrate among multiple requests corresponding to the same destination synchronous module.

5. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wicki et al. U.S. Patent 5,838,684 as applied to claim 18 and further in view of admitted prior art in the original disclosure.

Regarding claim 19, in column 10, lines 20-45, Wicki et al. teaches a plurality of arbiter subsystems, at least one arbiter subsystem dedicated to each output port. Wicki et al., however, does not teach arbitration circuitry comprising at least one Seitz arbiter. Admitted prior art in the original disclosure discloses implementations of Seitz arbiter and QFR circuits in C. L. Seitz, System Timing, chapter 7, pp. 218-262, Reading, Mass., Addison-Wesley, 1980, and F. U. Rosemberger, C. E. Molnar, T. J. Chaney, and T. P. Fang, Q-modules: Internally clocked delay-insensitive modules, IEEE Trans., Computers, vol. 37, no.9, pp. 1005-1018, September 1988, respectively; see column 54, line 23 via column 55, line 5, of the original disclosure. Because of known potential benefits of Seitz arbiter, one of ordinary skill in the art would have been motivated to implement Seitz arbiter, as taught by admitted prior art, into crossbar switch as taught by Wicki et al. in figure 1. Furthermore, implementation of new intended use (e.g. Seitz arbiter) for an old product does not make a claim to that old product patentable. In re Schreiber, 44 USPQ2d (Fed. Cir. 1997).

6. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wicki et al. U.S. Patent 5,838,684 as applied to claim 1 above, and further in view of Chou et al. U.S. Patent 6,763,418.

Regarding claim 24, Wicki et al. does not teach a build-in-self-test (BIST) module as set forth in the claim. Chou et al. discloses in figures 2A and 2B a data path 20 includes crossbar 22 to which eight communication ports 24 are coupled. Figure 2A shows an arbiter 36. In addition of eight communication ports 24, a management port 26 and a functional BIST port 28 are also coupled to crossbar 22; see figure 2B. Wicki et al. and Chou et al. teachings are in the same field of endeavor. Chou et al. invention differs from Wicki et al. invention in that Chou et al. teachings include a functional BIST port. In light of Chou et al. teachings, it would have been obvious for one of ordinary skill in the art at the time the invention was made that Wicki et al. crossbar switch can be modified to include a BIST as taught by Chou et al.. Motivation is that the BIST can be used for testing data transmission between the interfaces through crossbar switch.

7. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wicki et al. U.S. Patent 5,838,684 as applied to claim 1 above, and further in view of Barber et al. U.S. Patent 4,849,751.

Regarding claim 31, Wicki et al. does not teach the router system including crossbar switch is implemented on a CMOS integrated circuit as set forth in the application claim. Barber et al., nevertheless, teaches a CMOS integrated circuit digital crossbar switching arrangement shown in figure 5 of another US Patent. CMOS technology is mature and well known in the art. Because of the known benefits of CMOS technology, one of ordinary skill in the art at the time the invention was made would have been motivated to implement Wicki et al. router system including crossbar

unit on a CMOS integrated circuit as taught in Barber et al. invention. Wicki et al. teaches the router system can be on a semiconductor chip; see column 2, lines 1-6.

8. Claims 32-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wicki et al. U.S. Patent 5,838,684 as applied to claim 1 above, and further in view of Butts et al. U.S. Patent 6,002,861.

Regarding claim 32, Wicki et al. does not teach a computer-readable medium having data structures stored representative of the computer-bus switch architecture. However, as well known in the art of digital logic network design, one performs simulation of functional circuit design before actually building the digital logic network permanently. Butts et al. discusses such simulation in another US patent, wherein a method is disclosed for performing simulation of functional circuit design using a hardware and software emulation system. As disclosed in the abstract, Butts et al. teachings utilize a plurality of electronically reconfigurable gate array logic chips interconnected via a reconfigurable interconnect, which comprises a partial crossbar. The reconfigurable interconnect permits the digital network realized on the interconnected chips to be changed at will. Since Butts et al. teachings are in the same field of endeavor, and utilizes same components (e.g. logic chips, reconfigurable crossbar, ...) to simulate a digital network in the design, one of ordinary skill in the art would have been motivated to implement computer instructions stored a computer readable medium as data structures to simulate Wicki et al. et al. teachings, as part of the preliminary design before actual implementation.

Regarding claim 33, said claim is rejected on the same ground as for claim 32 because the claimed simulatable representation is discussed in claim 32.

Regarding claim 34, figure 43 in Butts et al. invention illustrates a block diagram of a Realizer design conversion system including netlists for logic chips. The Realizer design conversion system is part of hardware and software emulation system taught in Butts et al. invention.

Regarding claim 35, as recited in claim 32, Butts et al. discloses a method for performing simulation of a digital logic network as part of design using a hardware and software emulation system. In view of that, one of ordinary skill in the art would have recognized that the data structures as part of the hardware and software emulation system can be implemented to include code description representative of Wicki et al. teachings.

Regarding claim 36, using analogous argument as for claim 35, the code description would correspond to a hardware description language as part of the hardware and software emulation system.

Regarding claim 37, as discussed in claim 32, since Butts et al. teachings utilize a plurality of electronically reconfigurable gate array logic chips interconnected via a reconfigurable crossbar, corresponding to the claimed set of

semiconductor processing masks, it would have been obvious for one of ordinary skill in the art that the logic chips and reconfigurable crossbar as taught by Butts et al. can be implemented to represent at least a portion of Wicki et al. teachings.

Allowable Subject Matter

9. Claims 2-10, 14, 16-17, 20-23, 25-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

Khanh Cong Tran 06/24/2005
Examiner KHANH TRAN